Name: Class:

Task 1

1. Match up the registers on the left with the statements on the right.

|  |  |  |
| --- | --- | --- |
| Accumulator (ACC) |  | Points to the next instruction that needs to be executed. |
| Program Counter (PC) | Stores the memory address of the location in RAM that holds the data that needs to be fetched. Also stores the location in RAM that will be used to store data. |
| Memory Data Register (MDR) | Used for holding the actual instruction or data that is stored in RAM |
| Memory Address Register (MAR) | Used for temporarily storing arithmetic and logic results. |
| Current instruction register (CIR) |  | Used for holding the instruction that is currently being decoded and executed. |

(b) How does the computer know whether an address contains an instruction to be executed, or data to be used in an instruction?

Task 2

The segment of memory shown below stores both program instructions and data.

|  |  |
| --- | --- |
| **Address** | **Data / Instruction** |
| 101 | LDA #23 |
| 102 | SUB #20 |
| 103 | STO 206 |
| 104 |  |
| … | … |
| … | … |
| 205 | 9 |
| 206 |  |

(a) What is this architecture known as?

(b) With reference to the five CPU registers below, describe how they are used to complete the program instruction stored in location 101.

 LDA #23 means “Load the value 23”,

 SUB #20 means “subtract the value 20 from the accumulator”.

 STO 206 means “store the result in location 206”.

 Note the use of ‘#’ to denote an actual value rather than the value in a memory location.

 **Program Counter (PC)**

 **Memory Address Register (MAR)**

 **Memory Data Register (MDR)**

 **Accumulator**

(c) Complete the following series of steps:

 The PC holds the address 102 containing instruction SUB 20.

 Steps carried out in the Fetch-Execute cycle are labelled in sequence 1-7.

 At step 1: the address 102 is copied to the MAR.

 At step 2: the PC is incremented so it now holds 103.

 At step 3: the instruction at address 102 is copied to the MDR.

At step 4:

At step 5

At step 6:

At step 7: